Meir Fogel 19-03-2024

Operation of the A2D  
 for SPI HV , SPI \_SENSE , SPI ZCR

General Note

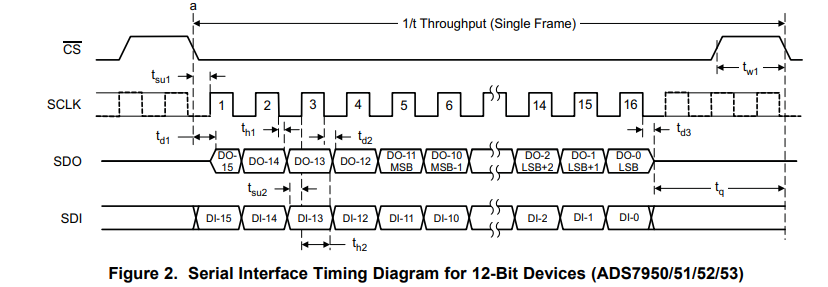
In this document

|  |  |
| --- | --- |
| **FPGA INPUT** | **FPGA OUTPUT** |
|  | CS |
| SDO | SCLK |
|  | SDI |

**Max SCLK frequency is 20Mhz**

**Maximum throughput rate is 1 Mhz using 20Mhz SCLK**

**TIMMING refer To ALL A2D**



SDI valid to **rising** edge of SCLK

SDO data bit valid to SCLK **falling**.

**SPI HV :**

.On poweron or after reset configure the HV A2D using

|  |  |
| --- | --- |
| cs | HV\_ADC\_CS\_fpga |
| sclk | HV\_ADC\_SCLK\_fpga |
| sdi | HV\_ADC\_SDI\_fpga |
| Sdo | HV\_ADC\_SDO\_fpga |

**Configuration**

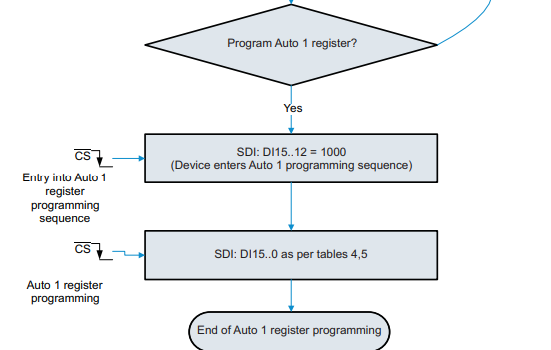
The configuration use 2 frames

Frame 1

|  |  |
| --- | --- |
| D15-12 | D11-0 are D.C. |
| 1000 | 0000 0000 0000 |

Frame 2

|  |
| --- |
| D15 -0 |
| F F F F |



**Sampling the HV A2D**

In the declare configuration above the A2D will sample all 8 channels start from channel 0 to channel 7  
 (to skip any channel you need write in the configuration frame 2 0 at the bit number mean FFFA mean channel 0 and 3 will be skipped)

Writing to the MODE CONTROL REGISTER of the A2D will create a conversion of current sampling channel and get the data on the SDO of the previous channel.

The SDO data includes the channel number of the included data.

The writing to the MODE CONTROL REGISTER is initialization and the data following the SDO at that frame is no meaning.

MODE CONTROL REGISTER

|  |
| --- |
| D15 -0 |
| 2 8 0 0 hex |

**SAMPLING CHANNELS NAMES**

|  |  |
| --- | --- |
|  |  |
| Cannel 0 | OUT4\_sns |
| Cannel 1 | Vsns\_PH1 |
| Cannel 2 | Vsns\_PH2 |
| Cannel 3 | Vsns\_PH3 |
| Cannel 4 | OUT4\_Isns |
| Cannel 5 | Vsns\_PH\_C\_RLY |
| Cannel 6 | Vsns\_PH\_B\_RLY |
| Cannel 7 | Vsns\_PH\_A\_RLY |

**SPI SENSE :**

.On poweron or after reset configure the HV A2D using

|  |  |
| --- | --- |
| cs | I\_sns\_ADC\_CS\_fpga |
| sclk | I\_sns\_ADC\_SCLK\_fpga |
| sdi | I\_sns\_ADC\_SDI\_fpga |
| Sdo | I\_sns\_ADC\_SDO\_fpga |

SDI valid to **rising** edge of SCLK

SDO data bit valid to SCLK **falling**.

**Configuration**

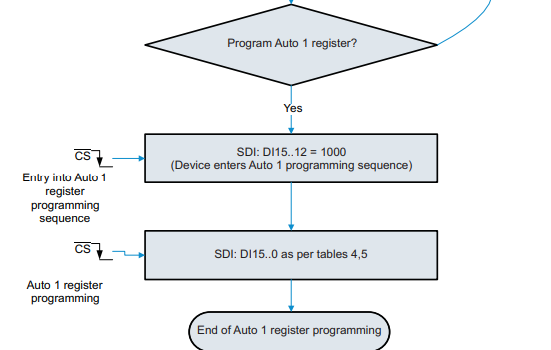
The configuration use 2 frames

Frame 1

|  |  |
| --- | --- |
| D15-12 | D11-0 are D.C. |
| 1000 | 0000 0000 0000 |

Frame 2

|  |
| --- |
| D15 -0 |
| F F F F |



**Sampling the SENSE**

In the declare configuration above the A2D will sample all 4 channels start from channel 0 to channel 3  
 (to skip any channel you need write in the configuration frame 2 0 at the bit number mean FFFA mean channel 0 and 3 will be skipped)

Writing to the MODE CONTROL REGISTER of the A2D will create a conversion of current sampling channel and get the data on the SDO of the previous channel.

The SDO data includes the channel number of the included data.

The writing to the MODE CONTROL REGISTER is initialization and the data following the SDO at that frame is no meaning.

MODE CONTROL REGISTER

|  |
| --- |
| D15 -0 |
| 2 8 0 0 hex |

**SAMPLING CHANNELS NAMES**

|  |  |
| --- | --- |
|  |  |
| Cannel 0 | DC\_PWR\_I\_sns |
| Cannel 1 | PH1\_I\_sns |
| Cannel 2 | PH2\_I\_sns |
| Cannel 3 | PH3\_I\_sns |

**SPI SENSE :**

.On poweron or after reset configure the HV A2D using

|  |  |
| --- | --- |
| cs | ZCR\_sns\_ADC\_CS\_fpga |
| sclk | ZCR\_sns\_ADC\_SCLK\_fpga |
| sdi | ZCR\_sns\_ADC\_SDI\_fpga |
| Sdo | ZCR\_sns\_ADC\_SDO\_fpga |

SDI valid to **rising** edge of SCLK

SDO data bit valid to SCLK **falling**.

**Configuration**

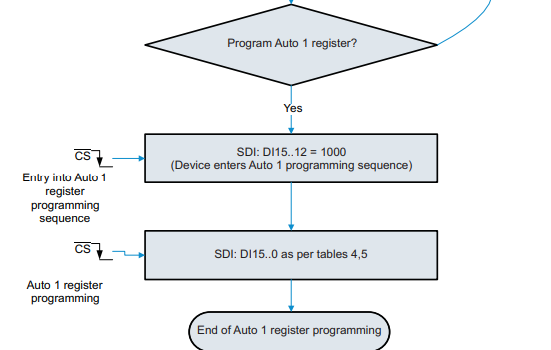
The configuration use 2 frames

Frame 1

|  |  |
| --- | --- |
| D15-12 | D11-0 are D.C. |
| 1000 | 0000 0000 0000 |

Frame 2

|  |
| --- |
| D15 -0 |
| F F F F |



**Sampling the ZCR**

In the declare configuration above the A2D will sample all 4 channels start from channel 0 to channel 3  
 (to skip any channel you need write in the configuration frame 2 0 at the bit number mean FFFA mean channel 0 and 3 will be skipped)

Writing to the MODE CONTROL REGISTER of the A2D will create a conversion of current sampling channel and get the data on the SDO of the previous channel.

The SDO data includes the channel number of the included data.

The writing to the MODE CONTROL REGISTER is initialization and the data following the SDO at that frame is no meaning.

MODE CONTROL REGISTER

|  |
| --- |
| D15 -0 |
| 2 8 0 0 hex |

**SAMPLING CHANNELS NAMES**

|  |  |
| --- | --- |
|  |  |
| Cannel 0 | DC\_PWR\_ZCR\_sns |
| Cannel 1 | PH1\_ZCR\_sns |
| Cannel 2 | PH2\_ZCR\_sns |
| Cannel 3 | PH3\_ZCR\_sns |